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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/647,080	09/26/2000	Jerome Meric	11345.017001	4075

22511 7590 08/12/2004

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EXAMINER	
LAMBRECHT, CHRISTOPHER M	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/647,080	MERIC ET AL.	
	Examiner	Art Unit	
	Christopher M. Lambrecht	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2, 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Hooper (Hooper et al., US005442390A).

With regard to claim 1, Hooper discloses a receiver/decoder (interface box 11, fig. 12) comprising: at least one port (network interface 801) for receiving messages (col. 14, ll. 35-37); a memory (segment cache 14) including a FIFO section (col. 15, ll. 33-34, where a circular buffer is a FIFO implementation of a buffer); at least one application module (decompressor/decoder 803); and FIFO control means (cache control 800) coupled (via 810 and 802) to the port (801), the memory (14) (cache control 800 is a subsystem of cache 14, see fig. 12, and hence is coupled thereto); and the application module (803, via 810, 300, and 820) operative in response to a message appearing at a port to write (performed by 810, upon receiving packet data, col. 15, ll. 21-25) the message into the FIFO section of the memory (segment cache 14) and to read (performed by 820) the message from the FIFO section of the memory out to (via line 807) an application module (803) (where cache controller 800 manages said reading and writing, col. 15, ll. 29-31).

As for claim 2, Hooper discloses a receiver/decoder according to claim 1 (see above) wherein the FIFO control means (800) is arranged to initiate reading out (by read controller 820) of a message (i.e., packetized video data) from the FIFO section of the memory (segment cache) to said application module

(803) before receipt of the message is complete (where the complete message constitutes a 1.2 GB feature length movie, col. 5, ll. 62-63, and segment cache has a storage capacity of 100 MB, col. 15, ll. 16-19, cache control 800 is inherently arranged to (capable of) initiate reading out of the message before receipt of the message is complete, as the entire message exceeds the capacity of the segment cache).

As for claim 3, Hooper discloses a receiver/decoder according to claim 1 wherein the FIFO control means (800) includes occupancy detector means for detecting the state of occupancy of the FIFO (segment cache 14) (cache controller 800 responds to "near-empty" condition, col. 15, ll. 37-47, relating to occupancy condition of the cache).

As for claim 13, Hooper discloses a broadcast system (VOD systems 20, fig. 1) comprising a receiver/decoder (interface 11, of customer premise equipment 10) according to claim 1 and means (communication network 30) for transmitting messages to the receiver/decoder.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hooper (Hooper et al., supplied by Applicant) in view of NEC (NEC Corporation, supplied by Applicant).

With regard to claim 4, Hooper discloses a receiver/decoder according to claim 3 wherein the occupancy detector means (800) is adapted to detect underflow of the FIFO (cache controller 800

responds to "near-empty" condition, col. 15, ll. 37-47, relating to occupancy condition of the cache). However, Hooper fails to explicitly disclose wherein the occupancy detector means is adapted to detect overflow of the FIFO (segment cache 14).

In an analogous art, NEC discloses occupancy detector means (buffer memory controller 101, fig. 2) adapted to detect overflow of a memory buffer (by monitoring outputs of comparators 1041-1044, col. 7, ll. 446-57), for the purpose of initiating overflow prevention processing for preventing overflow (col. 7, ll. 52-57).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper to include wherein the occupancy detector means is adapted to detect overflow of a memory buffer, as taught by NEC, for the purpose of preventing buffer overflow in a receiver/decoder.

As for claim 5, Hooper discloses a receiver/decoder according to claim 3. However, Hooper fails to explicitly disclose wherein the occupancy detector means is adapted to detect at least one threshold of impending overflow and underflow of the FIFO.

In an analogous art, NEC discloses occupancy detector means (memory buffer controller 101, fig. 2) adapted to detect at least one threshold (L1, L2, L3, and L4) of impending overflow and underflow of a memory buffer (col. 7, ll. 46-57), for the purpose of initiating underflow or overflow processing for preventing overflow or underflow (col. 7, ll. 52-57).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper to include wherein the occupancy detector means is adapted to detect at least one threshold of impending overflow and underflow of a memory buffer, as taught by NEC, for the purpose of preventing buffer underflow or overflow.

5. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hooper in view of RCA (RCA Thomson Licensing Corp., supplied by Applicant).

With regard to claim 6, Hooper discloses a receiver/decoder according to claim 1. However, Hooper fails to explicitly disclose, wherein the FIFO control means is arranged to flush a message from the FIFO section.

In an analogous art, RCA discloses a memory controller (275) arranged to flush a message from a memory buffer (col. 22, ll. 39-42), for the purpose of removing erroneous data from the memory (col. 22, ll. 33-36).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper to include a memory controller arranged to flush a message from a memory buffer, as taught by RCA, for the purpose of removing erroneous date from the memory buffer of a receiver/decoder.

With regard to claim 12, Hooper discloses a receiver/decoder according to claim 1 wherein a video device application unit (decomp/decode 803) unit fed from the FIFO section (segment cache 14). However, Hooper fails to disclose feeding a chip unit which is also fed with a video bit stream.

In an analogous art, RCA discloses a chip unit (transport processor 25, fig. 5) which is also fed with a bit stream (from buffers 23 and 24), for the purpose of providing error detection (col. 8, ll. 5-16).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper to include a chip unit which is also fed with a bit stream, as taught by RCA, for the purpose of providing error detection in a receiver/decoder.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hooper in view of Campanella (US005870390A) and Powell (US 4,835,733).

With regard to claim 7, Hooper discloses a receiver/decoder according to claim 1, comprising a FIFO buffer (segment cache 14, col. 33-34) and associated control means (800). However, Hooper fails to disclose a plurality of buffers and the control means comprises a respective plurality of buffer register control means.

In an analogous art, Campanella discloses a plurality of buffers (buffer pair 149 and 151, fig. 7), for the purpose of enabling an alternating fill pattern permitting continuous flow between the input and output of the buffers (col. 12, ll. 15-20). Campanella fails to explicitly disclose the control means comprises a respective plurality of buffer register control means.

Additionally, in an analogous art, Powell discloses the control means (access register unit 100, fig. 1) comprises a respective plurality of buffer register control means (registers START, STOP, IN PTR, and OUT PTR define address space boundaries, as well as read and write address for circular (FIFO) buffers in RAM 200, col. 4, ll. 24-31), for the purpose of enabling a memory device to function as a circular FIFO buffer (col. 4, ll. 15-36).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper to include a plurality of buffers, as taught by Campanella, and that the control means comprises a respective plurality of buffer register control means, as taught by Powell, for the purpose of enabling an alternating fill pattern permitting continuous flow between the input and output of the buffers and enabling a memory device to function as a circular FIFO buffer in a receiver/decoder.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hooper in view of Kutner (Kutner et al., supplied by Applicant).

With regard to claim 8, Hooper discloses a receiver/decoder according to claim 1, including a FIFO section (segment cache 14, implemented as a circular buffer, col. 15, ll. 33-34, where a circular buffer is an implementation of a is a FIFO buffer) and FIFO control means, as described above. However, Hooper fails to disclose the memory further includes (i.e., in addition to FIFO section and FIFO control means) a buffer section, and the receiver/decoder includes buffer control means operative in response to a message appearing at a port to write the message into the buffer section of the memory and in response to a control signal from an application module to read the message from the buffer to the application module.

In an analogous art, Kutner discloses a receiver/decoder includes a buffer section (641, fig. 7), and buffer control means (input control circuit 631 and output timing circuit 650) operative in response to a message appearing at a port to write the message into the buffer section (641) (col. 5, ll. 18-22) of the memory and to read the message from the buffer section (641) (col. 6, ll. 18-20) of the memory out to (via 652) an application module (660, col. 6, ll. 61-65), for the purpose of enabling the simultaneous receipt and storage of a plurality of video signals (col. 4, ll. 1-9).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper to further include a buffer section a buffer section, and buffer control means operative in response to a message appearing at a port to write the message into the buffer section of the memory and to read the message from the buffer section of the memory out to an application module, as taught by Kutner, for the purpose of enabling the simultaneous receipt and storage of a plurality of video signals in a receiver/decoder.

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hooper and Kutner as applied to claim 8 above, and further in view of Campanella and Powell.

With regard to claim 9, Hooper and Kutner together disclose the receiver/decoder of claim 8 (see above). However, Hooper and Kutner fail to disclose the buffer section (Kutner, 641, fig. 7) comprises two buffers areas defined by respective buffer registers in the buffer control means.

In an analogous art, Campanella discloses a buffer section (153, fig. 7) comprising a plurality of buffers (149 and 151, fig. 7), for the purpose of enabling an alternating fill pattern permitting continuous flow between the input and output of the buffers (col. 12, ll. 15-20). Campanella fails to explicitly disclose the control means comprises a respective plurality of buffer register control means.

Additionally, in an analogous art, Powell discloses the control means (access register unit 100, fig. 1) comprises a plurality of respective buffer registers (registers START, STOP, IN PTR, and OUT PTR define address space boundaries, as well as read and write address for circular (FIFO) buffers in RAM 200, col. 4, ll. 24-31), for the purpose of enabling a memory device to function as a circular FIFO buffer (col. 4, ll. 15-36).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper and Kutner to include a plurality of buffers, as taught by Campanella, and that the control means comprises a respective plurality of buffer register control means, as taught by Powell, for the purpose of enabling an alternating fill pattern permitting continuous flow between the input and output of the buffers and enabling a memory device to function as a circular FIFO buffer in a receiver/decoder.

As for claim 10, Hooper, Kutner, Campanella, and Powell together disclose the receiver/decoder according to claim 9 (see above). In addition, Campanella discloses the buffer control means (input

switch 161, fig. 7) is operable in a bit stream mode in which an incoming bit stream (incoming PRC symbols, col. 12, ll. 2-5) is directed into the currently selected buffer area and is then switched between the two buffer areas as each buffer area in turn becomes full (col. 12, ll. 15-25).

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hooper, Kutner, Campanella, and Powell as applied to claim 10 above, and further in view of O'Toole (O'Toole et al., US005828901A).

With regard to claim 11, Hooper, Kutner, Campanella, and Powell together disclose the receiver/decoder of claim 10. However, they fail to disclose the length of an incoming message is compared with the free space in the currently selected buffer area, and if that space is less than the length of the message, the other buffer is selected.

In an analogous art, O'Toole disclose the length of an incoming message (frame) is compared with the free space in the currently selected buffer (30, fig. 7) area (col. 9, ll. 58-60), and if that space is less than the length of the incoming message, the other buffer is selected (i.e., in order to store the remaining portion of the frame, col. 9, ll. 60-64, or in the case where the free space in the buffer is less than a minimum limit, the frame is stored entirely in a second buffer, col. 9, l. 65 – col. 10, l. 7), for the purpose of permitting multiple buffers to store long frames of data (col. 9, ll. 62-64).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Hooper, Kutner, Campanella, and Powell to include the length of an incoming message is compared with the free space in the currently selected buffer area, and if that space is less than the length of the incoming message, the other buffer is selected, as taught by O'Toole, for the purpose of permitting multiple buffers to store long frames of data in a receiver/decoder.

Conclusion

10. The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually depositing or transmitting the correspondence or by an individual who, upon information and belief, expects the correspondence to be mailed or transmitted in the normal course of business by another no later than the date indicated.

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Please refer to 37 CFR 1.6(d) and 1.8(a)(2) for filing limitations concerning facsimile transmissions and mailing, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Lambrecht whose telephone number is (703) 305-8710. The examiner can normally be reached on 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christopher Grant can be reached on (703) 305-4755. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher M. Lambrecht
Examiner
Art Unit 2611

CML

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PRIMARY EXAMINER